Mustafa Munawar Shihab

7421 Frankford Road Apt 1431, Dallas, TX 75252 | Cell: +1 (334) 444 - 1371 | E-mail: mustafa.shihab@utdallas.edu
LinkedIn: https://www.linkedin.com/in/mustafa-shihab | Website: http://www.mustafashihab.com

Education

PhD in Electrical Engineering 2014 - Present
The University of Texas at Dallas – Richardson, Texas CGPA: 4.00/4.00
Advisor: Dr. Yiorgos Makris
Dissertation: *Enabling Hardware Security and In-Field Hardware Update Through a Novel Hybrid IC Design Methodology*

MS in Electrical Engineering 2011 - 2013
Auburn University – Auburn, Alabama CGPA: 3.88/4.00
Advisor: Dr. Vishwani Agrawal
Thesis: *A High-Voltage On-Chip Power Distribution Network*

BS in Electronic and Telecommunication Engineering 2004 - 2008
North South University – Dhaka, Bangladesh CGPA: 3.80/4.00
Senior Project: *A Comparative Study of the New 5T and the Standard 6T SRAM Designs - A possible solution towards High-Density SRAMs*

Key Areas of Interest and Expertise

Computer Architecture, Hardware Security, Reconfigurable Computing, Non-Volatile Memory

Publications

Peer-Reviewed Journals

[J2] Monir Zaman, **Mustafa M. Shihab**, Ayse K. Cuskun, and Yiorgos Makris, "*CAPE: A cross-layer framework for accurate microprocessor power estimation*" – Integration - The VLSI Journal, Elsevier, 2019.

[J1] **Mustafa M. Shihab**, Jie Zhang, Mahmut Kandemir, and Myoungsoo Jung, "*ReveNAND: A Fast-Drift Aware Resilient 3D NAND Flash*" – ACM Transactions on Architecture and Code Optimization (TACO) – Vol. 15-2, 2018.

Conference/Workshop Papers

[C16] **Mustafa M. Shihab**, Bharath Ramanidharan, Gaurav R. Reddy, Jingxian Tian, William Swartz Jr., Benjamin C. Schaefer, Carl Sechen, and Yiorgos Makris, "*CASPER: CAD Framework for a Novel Transistor-Level Programmable Fabric*" – IEEE ISCAS 2020 (Accepted).

[C15] **Mustafa M. Shihab**, Bharath Ramanidharan, Suraag S. Tellakula, Gaurav R. Reddy, Jingxian Tian, Carl Sechen, and Yiorgos Makris, "*ATTEST: Application-Agnostic Testing of a Novel Transistor-Level Programmable Fabric*" – IEEE VTS 2020.

[C14] Bo Hu, **Mustafa M. Shihab**, Yiorgos Makris, Benjamin C. Schaefer, and Carl Sechen, "*An Efficient MILP-Based Aging-Aware Floorplanner for Multi-Context Coarse-Grained Runtime Reconfigurable FPGAs*" – IEEE/ACM DATE 2020.

[C13] Bo Hu, **Mustafa M. Shihab**, Yiorgos Makris, Benjamin C. Schaefer, and Carl Sechen, "*Extending the Lifetime of Coarse-grained Runtime Reconfigurable FPGAs by Balancing Processing Element Usage*" – IEEE FPT 2019.

[C12] Bo Hu, Jingxian Tian, **Mustafa M. Shihab**, Gaurav R. Reddy, William Swartz Jr., Benjamin C. Schaefer, Carl Sechen, and Yiorgos Makris, "*Functional Obfuscation of Hardware Accelerators through Selective Partial Design Extraction onto an Embedded FPGA*" – ACM GLSVLSI 2019.

[C11] **Mustafa M. Shihab**, Jingxian Tian, Gaurav R. Reddy, Bo Hu, William Swartz Jr., Benjamin C. Schaefer, Carl Sechen, and Yiorgos Makris, "*Design Obfuscation through Selective Post-Fabrication Transistor-Level Programming*" – IEEE/ACM DATE 2019.

[C10] **Mustafa M. Shihab**, Jie Zhang, Mahmut Kandemir, and Myoungsoo Jung, "*Addressing Fast-Detrapping for Reliable 3D NAND Flash Design*" – NVMW 2019 [Memorable Paper Award Finalist].

[C9] **Mustafa M. Shihab** and Vishwani Agrawal, "*Energy Efficient Power Distribution on Many-Core SoC*" – IEEE VLSID 2019.

[C8] Monir Zaman, **Mustafa M. Shihab**, Ayse K. Cuskun, and Yiorgos Makris, "*Towards a Cross-Layer Framework for Accurate Power Modeling of Microprocessor Designs*" – IEEE PATMOS 2018.

[C7] **Mustafa M. Shihab**, Jie Zhang, Joseph Callenes-Sloan, and Myoungsoo Jung, "*Couture: Tailoring STT-MRAM for Persistent Main Memory*" – USENIX INFLOW 2016.

[C6] **Mustafa M. Shihab**, Myoungsoo Jung, and Joseph Callenes-Sloan, "*SpinDIMM: A Reliable Memory Design with Tailored STT-MRAM and Reinforcement Learning*" – IEEE SELSE 2016.

[C5] Jie Zhang, Gieseo Park, **Mustafa M. Shihab**, David Donofrio, John Shalf, and Myoungsoo Jung, "*OpenNVM: An Open-Sourced FPGA-based NVM Controller for Memory Characterization*" – IEEE ICCD 2015.

[C4] Gieseo Park, **Mustafa M. Shihab**, Lubaba Nahar, Wonil Choi, David Donofrio, John Shalf, and Myoungsoo Jung, "*NVM- Charade: An Open-Sourced FPGA Based NVM Characterization Scheme*" – IEEE/ACM WARP (ISCA) 2015.

[C3] **Mustafa M. Shihab**, Karl Taht, and Myoungsoo Jung, "*GPUdrive: Reconsidering Storage Accesses for GPU Acceleration*" – IEEE/ACM ABSD (ISCA) 2014.

[C2] Youngbin Jin, **Mustafa M. Shihab**, and Myoungsoo Jung, "*Exploring Area, Power and Latency Dynamics of STT-MRAM to Substitute for Main Memory*" – IEEE/ACM Memory Forum (ISCA) 2014.

[C1] Jie Zhang, **Mustafa M. Shihab**, and Myoungsoo Jung, "*Power, Energy and Thermal Considerations in SSD-Based I/O Acceleration*" – USENIX HotStorage 2014.

Professional Experience

Department of Electrical Engineering – The University of Texas at Dallas
Graduate Research Assistant (GRA) May 2015 – Present
Responsibility: Perform individual and collaborative research on hardware security, reconfigurable computing, emerging non-volatile memory technologies, and develop required architectural support for their reliable implementation.

Software Services Group – Intel Corporation (Santa Clara, CA)
Software Engineer - Graduate Intern June 2016 – December 2016
Responsibility: Leverage a wide range of microarchitecture dependent and independent metrics to predict system performance for applications from client, cloud, and HPC domains. Also extended the current profiling methodology for specific set of workloads running on Mac OS.

Department of Electrical Engineering – The University of Texas at Dallas
Graduate Teaching Assistant (GTA) August 2014 – May 2015
Courses: Computer Architecture, Microprocessor Systems

Department of Electrical & Computer Engineering - Auburn University
Graduate Research Assistant (GRA) August 2012 – July 2013
Responsibility: Worked on open problems in low-power VLSI design/testing that culminated in the MS thesis.

Micro-Fabrication Laboratory - Alabama Microelectronics Science and Technology Center (AMSTC)
Research Assistant (GRA)/Student Process Engineer May 2011 - July 2013
Responsibility: Assisted in managing the 4000 sq. ft. Class-100 Clean-Room with a wide range of equipment.

Augere Wireless Broadband Bangladesh Limited
Support Engineer September 2009 – September 2010
Worked in the core troubleshooting team as the liaison between the marketing and the technical department of the company for resolving concerns and disparities.

Department of Electrical Engineering and Computer Science - North South University
Lab Instructor and Teaching Assistant May 2007 – May 2009
Courses: Introduction to VLSI, Verilog HDL, Microprocessors and Assembly Language.

Technical Skills

Programming Languages: Python, **Verilog**, C, C++, VHDL
Hardware Design & Simulation: ModelSim, gem5, McPAT, LTspice, MATLAB
CAD Implementation: Synopsys DC, Xilinx Vivado, Intel Quartus, Mentor Precision RTL, TimberWolf, VPR
Operating Systems: Microsoft Windows, Linux, Mac OS

Achievements and Involvements

- Received *Graduate Fellowship* from Auburn University
- Received the distinction of *Summa Cum Laude* from North South University